DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will now be described in detail with reference to the accompanying drawings.

FIG. 1 is a block diagram illustrating a nonvolatile semiconductor memory device according to an embodiment of the present invention. The nonvolatile semiconductor memory device of FIG. 1 includes a nonvolatile memory cell array 10, a column decoder 12, a row decoder 14, a sense amplifier 16, a write driver 18, a data output buffer 20, a data input buffer 22, a program detecting circuit 24, and a controller 26.

Functions of the above-referenced components of the nonvolatile semiconductor memory device of FIG. 1 are explained below.

The nonvolatile memory cell array 10 includes a one-time programming ("OTP") region and a normal region. Data can be written to the OTP region only one time and is accessed by a word line selecting signal WL1. Data written to the normal region may be written or read repeatedly and accessed by word line selecting signals WL2 to WLn. The column decoder 12 decodes a column address Y to generate column selecting signals Y1 to Ym. The row decoder 14 decodes a row address X to generate the word line selecting signals WL1 to WLn. The sense amplifier 16 amplifies a signal "do" output from the nonvolatile memory cell array 10 and generates amplified data "ddo" in response to a sense amplifier enable signal MSAEN. The write driver 18 writes buffered data "ddi" in the nonvolatile memory cell array 10 in response to a write driver enable signal WDEN. The data output buffer 20 buffers the amplified data "ddo" to generate output data DO in response to a data output enable signal DOEN. The data

input buffer 22 buffers input data DI to generate to the buffered data "ddi" in response to a data input enable signal DIEN. The program detecting circuit 24 compares the amplified data "ddo" to generate a comparison detecting signal DET in response to a signal DIS. The controller 26 is enabled when an inverted chip enable signal CEB having a logic "low" level is applied. The controller 26 activates the sense amplifier enable signal MSAEN for a read operation when an inverted write enable signal WEB having a logic "high" level is applied. The controller 26 activates the data output enable signal DOEN when an inverted output enable signal OEB having a logic "low" level is applied. Also, the controller 26 inactivates the signal DIS when the inverted write enable signal WEB having a logic "low" level and a specific mode signal TM having a logic "low" level are applied. The controller 26 activates the data input enable signal DIEN and the sense amplifier enable signal MSAEN when the inverted write enable signal WEB having a logic "low" level, the specific mode signal TM having a logic "high" level, and the word line selecting signal WL1 are applied. The controller 26 activates the write driver enable signal WDEN in response to the comparison detecting signal DET.

The nonvolatile semiconductor memory device of FIG. 1 detects whether the OTP region of the nonvolatile memory cell array 10 is programmed during a write operation by the program detecting circuit 24. Inherent data is written to the OTP region if data is not recorded in the OTP region. Inherent data cannot be written in the OTP region if data is already recorded.

FIG. 2 is a flow chart illustrating a method of writing data in the one-time programming region of the nonvolatile semiconductor memory device of FIG. 1.

First, a semiconductor manufacturer applies the inverted chip enable signal CEB having a logic "low" level to the nonvolatile semiconductor memory device (step 100), whereby an operation of the nonvolatile semiconductor memory device is enabled.

Next, the semiconductor manufacturer applies the inverted write enable signal WEB having a logic "low" level to the nonvolatile semiconductor memory

device (step 110). When the inverted write enable signal WEB having a logic "low" level is applied, the controller 26 activates a data input enable signal DIEN.

If the inverted write enable signal WEB does not have a logic "low" level, a read operation is performed (step 120). That is, when the inverted write enable signal WEB having a logic "high" level is applied, the controller 26 activates the sense amplifier enable signal MSAEN and the data output enable signal DOEN.

If the inverted write enable signal WEB having a logic "low" level is applied, it is determined whether or not a specific mode signal TM has a logic "low" level (step 130). If the specific mode signal TM has a logic "high" level, a write operation is performed (step 140). However, if the specific mode signal TM has a logic "low" level, certain data is written in the OTP region of the nonvolatile memory cell array 10 of FIG. 1 (step 150).

In more detail, the controller 26 inactivates a signal DIS in response to the specific mode signal TM having a logic "low" level. The row decoder 14 decodes a row address X to activate a word line selecting signal WL1, and the column decoder 12 decodes the column address Y to generate one of the column selecting signals Y1 to Ym to access the OTP region. The data input buffer 22 buffers and outputs externally input data, and the write driver 18 applies the buffered data to the nonvolatile memory cell array 10, whereby certain data is written in the OTP region of the nonvolatile memory cell array 10 of FIG. 1. By repeatedly performing the method described above while changing the column

address Y, certain data is written in the OTP region of the nonvolatile memory cell array 10.

When a power voltage is applied to a power voltage applying pad after certain data is written in the OTP region of the nonvolatile memory cell array 10, a specific mode signal TM connected to the power voltage applying pad is enabled.

FIG. 3 is a flow chart illustrating the one-time programming control method of the nonvolatile semiconductor memory device of FIG. 1. In particular, FIG. 3 shows an operation of the step 140 of FIG. 2.

The X and Y addresses and data are inputted (step 300). The row decoder 14 decodes the row address X to select one of the word line selecting signals WL1 to WLn, and the column decoder 12 decodes the column address Y to select one of the column selecting signals Y1 to Ym.

The controller 26 determines whether the word line selecting signal WL1 is activated (step 310).

If the word line selecting signal WL1 is not activated, the controller 26 inactivates the sense amplifier enable signal MSAEN and the signal DIS in response to the word line selecting signal WL1 (step 320).

If the word line selecting signal WL1 is activated, the controller 26 activates the sense amplifier enable signal MSAEN and the signal DIS in response to the word line selecting signal WL1 (step 330).

The program detecting circuit 24 compares data "ddo" output from the sense amplifier 16 to generate the comparison detecting signal DET (step 340). The program detecting circuit 24 compares whether data "ddo" output from the sense amplifier 16, i.e.,

data read from the OTP region, are all "0" (or "1"). If the data are all "0" (or "1"), the program detecting circuit 24 activates a comparison detecting signal DET. In other cases, the comparison detecting signal DET is inactivated.

The controller 26 determines whether the comparison detecting signal DET is activated (step 350).

If the comparison detecting signal DET is activated, the controller 26 activates the write driver enable signal WDEN (step 360). Also, the step 360 is performed after the step 320.

On the other hand, if the comparison detecting signal DET is inactivated, the controller 26 inactivates the write driver enable signal WDEN (step 370). Subsequent to the step 360, operation of the write driver 18 is enabled, so that buffered input data "ddi" output from the data input buffer 22 is written in the nonvolatile memory cell array 10 of FIG. 1 (step 380).

In the step 300, the X and Y addresses and data are simultaneously applied, but the X and Y addresses and data can be sequentially applied.

In the embodiment described above, the nonvolatile semiconductor memory device of FIG. 1 and one-time programming control circuit activate the write driver enable signal WDEN to write data in the normal region of the nonvolatile memory cell array 10 when the normal region is selected during a write operation. When the OTP region is selected, the sense amplifier enable signal MSAEN is activated to determine whether inherent data is programmed in the OTP region, and the signal DIS is activated, so that operation of the program detecting circuit 24 is enabled. If inherent data is programmed, the controller 26 inactivates the write driver enable signal WDEN. If

inherent data is not programmed, the controller 26 activates the write driver enable signal WDEN to write inherent data in the OTP region.

FIG. 4 is a block diagram illustrating a nonvolatile semiconductor memory device according to another embodiment of the present invention. The nonvolatile semiconductor memory device of FIG. 4 includes a nonvolatile memory cell array 10', a column decoder 12, a row decoder 14, a sense amplifier 16, a write driver 18, a data output buffer 20, a data input buffer 22, first and second program detecting circuits 24-1 and 24-2, and a controller 26'.

The nonvolatile semiconductor memory device of FIG. 4 has the first and second program detecting circuits 24-1 and 24-2 and the controller 26' instead of the program detecting circuit 24 and the controller 26, respectively. The nonvolatile memory cell array 10' includes a normal region, an OTP region and a ~~parity~~ lock bit region, unlike the nonvolatile memory cell array 10 of FIG. 1 having the normal region and the OTP region.

Functions of components of the nonvolatile semiconductor memory device of FIG. 4 are explained below. In FIGs. 1 and 4, like reference numerals denote like parts and perform like operations, and thus functions of added or changed components are explained below.

In the nonvolatile memory cell array 10', the one-time programming (OTP) region and the ~~parity~~ lock bit region are accessed by a word line selecting signal WL1, and the normal region is accessed by word line selecting signals WL2 to WLn. Inherent data can be programmed in the OTP region only one time. ~~Parity d~~Data "0" (or "1") is written to the ~~parity~~ lock bit region when the certain data are completely stored in the OTP region.

The first program detecting circuit 24-1 is enabled in response to a signal DIS1 to detect whether data of the ~~parity~~ lock bit region output from the sense amplifier 16 is "0" (or "1") to generate a first comparison detecting signal DET1. The second program detecting circuit 24-2 is enabled in response to a signal DIS2 to detect whether data output from the sense amplifier 16 are all "0" (or "1") to generate a second comparison detecting signal DET2.

The controller 26' is enabled when an inverted chip enable signal CEB having a logic "low" level is applied. The controller 26' activates a sense amplifier enable signal MSAEN for a read operation when an inverted write enable signal WEB having a logic "high" level is applied. The controller 26' activates a data output enable signal DOEN when an inverted output enable signal OEB having a logic "low" level is applied. Also, the controller 26' inactivates signals DIS1 and DIS2 when the inverted write enable signal WEB having a logic "low" level and a specific mode signal TM having a logic "low" level are applied. The controller 26' activates a data input enable signal DIEN, the sense amplifier enable signal MSAEN and the signal DIS1 when the inverted write enable signal WEB having a logic "low" level, a specific mode signal TM, and a word line selecting signal WL1 having a logic "high" level are applied. The controller 26' activates the signal DIS2 when the signal DET1 is activated.

The nonvolatile semiconductor memory device of FIG. 4 determines whether the OTP region is programmed using data of the ~~parity~~ lock bit region to generate a first comparison detecting signal DET1, and then determines whether the OTP region is programmed using data of the OTP region to generate a second comparison detecting signal DET2. Therefore, if it is determined that the OTP region has been programmed one time, a write driver enable signal WDEN is inactivated, thereby preventing data from being written in the OTP region.

FIG. 5 is a flow chart illustrating a method of writing data in the one-time programming region of the nonvolatile semiconductor memory device of FIG. 4.

Steps of like reference numerals in FIGs. 2 and 5 perform like operations. The methods of FIGs. 2 and 5 differ in steps 150 and 200.

In the step 200, certain data is written in the OTP region of the nonvolatile memory cell array 10', and when data is completely written in the OTP region, ~~parity~~ lock data "0" (or "1") is written in the ~~parity~~ lock bit region.

That is, after the certain data "0" (or "1") is written in the OTP region of the nonvolatile memory cell array 10' by the same way as the step 150 of FIG. 2, the ~~parity~~ lock data "0" (or "1") is written in the ~~parity~~ lock bit region.

FIG. 6 is a flow chart illustrating a one-time programming control method of the nonvolatile semiconductor memory device of FIG. 4. In particular, FIG. 6 shows operation of the step 140 of FIG. 5.

The X and Y addresses and data are inputted (step 400). The row decoder 14 decodes the row address X to select one of the word line selecting

signals WL1 to WLn, and the column decoder 12 decodes the column address Y to select one of the column selecting signals Y1 to Ym.

The controller 26' determines whether the word line selecting signal WL1 is activated (step 410).

If the word line selecting signal WL1 is not activated, the controller 26' inactivates the sense amplifier enable signal MSAEN and inactivates signals DIS1 and DIS2 (step 420).

If the word line selecting signal WL1 is activated, the controller 26' activates the sense amplifier enable signal MSAEN and activates the signal DIS1 (step 430).

The first program detecting circuit 24-1 compares a ~~parity~~ lock bit output from the sense amplifier 16 to generate the first comparison detecting signal DET1 (step 440). For example, the first program detecting circuit 24-1 compares whether data read from the ~~parity~~ lock bit region is "0"(or "1"). If the data is "0" (or "1"), the first comparison detecting signal DET1 is activated. If the data is "1", the first comparison detecting signal DET1 is inactivated.

The controller 26' determines whether the first comparison detecting signal DET1 is activated (step 450).

If the first comparison detecting signal DET1 is not activated, the controller 26' inactivates the write driver enable signal WDEN (step 460).

On the other hand, if the first comparison detecting signal DET1 is activated, the controller 26' activates the signal DIS2 (step 470).

The second program detecting circuit 24-2 compares data output from the sense amplifier 16 to generate the second comparison detecting signal DET2 (step 480). For example, the second program detecting circuit 24-2 is enabled in response to the signal DIS2 to compare whether data read from the OTP region are all "0" (or "1"). If the data are all "0" (or "1"), the second comparison detecting signal DET2 is activated. In other cases, the second comparison detecting signal DET2 is inactivated.

The controller 26' determines whether the second comparison detecting signal DET2 is activated (step 490).

If the second comparison detecting signal DET2 is not activated, the step 460 is performed. For example, the controller 26' inactivates the write driver enable signal WDEN.

On the other hand, if the second comparison detecting signal DET2 is activated, the controller 26' activates the write driver enable signal WDEN (step 500). Also, the step 500 is performed after the step 420.

Then, operation of the write driver 18 is enabled in response to a write driver enable signal WDEN, thereby writing data in the nonvolatile memory cell array 10' (step 510).

In the nonvolatile semiconductor memory device of FIG 4, when the OTP region of the nonvolatile memory cell array 10' is selected and one bit or a predetermined bit of data is read, a ~~parity~~ lock bit data of the ~~parity~~ lock bit region is simultaneously selected to be output to the sense amplifier 16.

Also, when the OTP region is selected and one bit or a predetermined bit of data is read after the one-time programming is performed in the OTP region, one bit or a predetermined bit of data "0" (or "1") is stored "as is". In this case, the nonvolatile semiconductor memory device of FIG. 1 can not protect inherent data stored in the OTP region because the program detecting circuit activates a comparison detecting signal to enable the write driver enable signal WDEN. However, even in the case that one bit or a predetermined bit of data "0" (or "1") is stored "as is", the nonvolatile semiconductor memory device of FIG. 4 can protect inherent data safely because the write driver enable signal WDEN is enabled only when the first comparison detecting circuit compares the ~~parity~~ lock bit to activate a first comparison detecting signal, and then the second comparison detecting circuit compares data stored in the OTP region to activate a second comparison detecting signal.

In accordance with at least one embodiment of the present invention, the one-time programming control method of the nonvolatile semiconductor memory device of the present invention can be applied to semiconductor memory devices having a nonvolatile memory cell array which perform a write operation and a read operation and do not need to perform an erase operation.

It should be appreciated that, in the nonvolatile semiconductor device described above, the program detecting circuit may be included in the control means.

As described herein before, the nonvolatile semiconductor memory device of the present invention and the one-time programming control method thereof, which do not need to perform an erase operation, can safely protect inherent data stored in the one-time programming region of a nonvolatile memory cell array.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

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